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EXAMINER

TM02/0801

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ART UNIT	PAPER NUMBER
2187	4

DATE MAILED: 08/01/01

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), _____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☑ Claims 1-3 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☑ Claims 1-3 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☑ The proposed ~~additional or~~ substitute sheet(s) of drawings, filed on 8-22-00 has (have) been ☐ approved by the examiner; ☑ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

AO

PTOL-326 (Rev. 2/93)

☆ U.S. GOVERNMENT PRINTING OFFICE: 1995-391-982

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. A new title such as --Programmable System Including Self Locking Memory Circuit For a Tristate Data Bus-- is suggested (see claim 1, line 1 and claim 2, lines 1, 4-5 and 9, e.g.). The loss in brevity of title is more than offset by the gain in its informative value in indexing, classifying, searching, etc. See MPEP 606 and 606.01.

2. The abstract of the disclosure is objected to because it does not enable one to quickly determine from a cursory inspection the nature and gist of the technical disclosure as required by 37 CFR 1.72(b). It appears in line 1, language such as --programmable system and a-- should be inserted after "A"m in line 1 for clarity. Also, it appears "each bit line" in line 3 should be changed to –one of the bit lines– for clarity and consistency ("a ... buffer chip for connection to each bit line" is somewhat confusing. Also note claim 1, lines 4-5.). Additionally, it appears one or two sentences should be added describing additionally claimed and disclosed features for clarity and completeness. [For example, in line 9 (page line 10), after "circuit.", insert a sentence such as --The tristate data bus may be connected between a digital signal processor (DSP), a complex programmable logic device (CPLD) and a central processing unit (CPU) operating at different rates or speeds.-- See claims 2 and 3, e.g.]

Appropriate correction is required. See MPEP § 608.01(b).

3. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on August 24, 2000, have been disapproved by the Examiner.

The drawings are objected to because in Figure 2, it appears "DATE" (both occurrences) should be –DATA– for clarity and consistency.

Also, in Figures and 1B, the notation "0" at the end of each of the write and read inputs and outputs is somewhat confusing and not entirely understood. [Is this a port number? A bit number, i.e. should the "0" in the second through eighth inputs/outputs in each column be changed to 1 to 7, respectively? In this regard, also see page 5, lines 19-21 and page 5, lines 17-18, e.g.]

Also in Figure 1A, it appears one of the circuits 220 should be enclosed within a dashed box, with a short curved line extending from the reference numeral 220 to the dashed box, for clarity.

Also in Figures 1A and 1B, as well as Figure 2, it appears a representative one of the "boxes" 22, 26 and 32 should be labeled for clarity (i.e., either a descriptive label such as –Int. Imped.-- or a symbol such as a dashed resistor added within one of the boxes, with the reference numeral 26 (22) be placed outside the box, for clarity.

Applicant is REQUIRED to submit a proposed drawing correction in response to this Office action. However, actual formal correction of the noted defect(s) can be deferred until the application is allowed by the examiner.

Also note MPEP 608.02(r) and (v).

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the central processing unit (CPU) of claims 2 and 3, and the complex programmable logic device of claim 3, must be shown or the features canceled from the claims. No new matter should be entered.

5. The disclosure has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

On page 1, line 3, the wording "relates to" is somewhat confusing as it is not entirely whether priority is being claimed from the provisional application. If priority is desired, it appears a specific claim should be made [e.g., "relates to" changed to –claims priority under 35 U.S.C. 119(e) from-- or other similar language), and the heading ("Cross Reference ...") deleted]. See MPEP 201.11, e.g. Note also that the provisional application does not appear to have been listed in the oath/declaration. Updated information (Serial No., updated status, if appropriate, etc.) should also be provided if the application is simply "related."

On page 1, line 17, and throughout the specification, the first occurrence of all acronyms or abbreviations should be written out for clarity, whether or not they may be considered "well

known." Accordingly, it appears "CPU" should be changed to –central processing unit (CPU)-- for clarity.

On page 1, lines 20-21, "and low impedance state" is not clear in this context. In line 22, it appears "line" should be –line,-- for clarity.

On page 2, line 21, it appears "supplying circuit" should be changed to –supply device or circuit– for clarity and consistency (note the use of "device" in lines 14 and 16, e.g.). In line 24, it appears –the latching circuit of– should be inserted before "the invention" for clarity and consistency (see line 17, as well as page 3, line 14, e.g.).

On page 3, line 12, it appears –provisional– should be inserted before "patent" for clarity and consistency (note page 1, line 3, e.g.). See also page 5, line 26. In line 24, "from in" appears to read more clearly as simply –from–.

On page 5, line 14, it appears "such" should be –the–. Also, "circuit of the invention" in lines 14-15 appears to read more clearly as -- latching circuit of the present invention–. In line 19, it appears "Figure 1 thereof shows" should be changed to –Figures 1A and 1B together show- - for clarity and consistency (with the formal drawings filed August 24, 2000).

On page 8, line 20, "monetarily" is unclear in this context (–momentarily–?).

On page 9, line 8, "hunt" is not entirely clear here. It appears an explanatory sentence or parenthetical phrase should be added explaining what is meant by "hunt" in this context. In line 24, it appears "noted, above the CPU" should be –noted above, the CPU– for clarity.

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected.

In the claims:

In claim 1, line 7, it appears "and" should be moved after "lines;" in line 5 for clarity.

In claim 2, it appears "CPU; said" in lines 5-6 should be changed to –CPU, said–, and "functions," in line 8 changed to –functions;-- for clarity. In line 6, it appears "difference" should be changed to –different– for clarity.

In claim 3, line 3, it appears –(CPLD)-- should be inserted after "device" for clarity.

Appropriate correction is required.

6. It is noted here that this application appears to contain claims directed to distinct inventions.

More specifically, claim 1 sets forth a "self-locking memory circuit" for a tri-state data bus, which appears to be a subcombination of the "programmable system" of claims 2 and 3, which programmable system includes "self-locking data bus circuits." [In this regard, also see MPEP 806.05(c).] However, combination claims 2 and 3 not setting forth the details of the subcombination claim appear to provide evidence that the combination as claimed does not require the particulars of the subcombination for patentability. Additionally, the subcombination appears to have separate utility such as a self-locking memory circuit for different circuits in a

computer or data processing system (in this regard, also see page 2, lines 1-5 and page 6, lines 2-5 of the specification).

Again, while these inventions appear to be distinct, a restriction requirement is NOT being made at this time since it does not appear there will be a substantial burden on the Office if restriction is not required, given that there is only one claim in the first group and only two claims in the second group, and since the searches for the different groups overlap to some extent. However, restriction may be required in the future depending on how the claims are amended. In this regard, also see MPEP 811.

7. Claims 1-3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, the wording "said chip and resistor having upper and lower voltage thresholds" is confusing. Also, in lines 9-11, the wording "when a level ... passes through said thresholds" is somewhat confusing. It appears "said chip and resistor having" in line 8 should be changed to –wherein the circuit has-- or other similar language, and –one of– inserted after "through" in line 10, for clarity and consistency. See page 6, line 21; page 7, line 18; page 8, line 14; and page 9, lines 0-10, e.g.).

In claims 2 and 3, it is not entirely clear from the claim language how the self-locking data bus circuits "match" the different operating rates.

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Buch.

With respect to claim 1, Buch discloses a "self locking" memory or bus latching circuit for a tri-state data bus having multiple bit or data lines, the memory or latching circuit including a non-inverting buffer chip (64, 66 together, e.g., in Figure 5) for connection to one of the bit or data lines, and a resistor (68 in Fig. 5, e.g.) having a predetermined electrical resistance connected across the buffer chip. [Note that while two inverters are shown in Figure 5, Buch also specifically teaches that a non-inverting amplifier may be used in place of the pair of inverters 64, 66 (see column 5, lines 60-62, e.g.)]

The memory or bus latching circuit maintains or stores the level of data on the bus until a subsequent data or voltage level is driven onto the data bus. The resistance value may be chosen to adjust the thresholds at which the circuit will change state. In this manner, the memory or latching circuit has upper and lower "threshold" voltage thresholds that cause the buffer chip or latching circuit to change states when a level of voltage applied to the chip and the resistor

"passes through" one of the thresholds. The memory or latching circuit is "self-locking" and does not change state until a voltage is again applied to the data bus which "passes through" one of the thresholds. See column 5, lines 31-35; column 5, line 56 to column 6, line 2; column 6, line 61b to column 7, line 5; and Figure 5, for example..

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buch.

With respect to claims 2 and 3, Buch discloses a "programmable" computer system including a tri-state data bus electrically connected to a central processing unit (CPU), and a plurality of "self-locking" data bus latching or memory circuits connected to respective bit or data lines of the data bus.

Buch teaches that the "self locking" data bus latching circuit may include a non-inverting buffer chip and a resistor having a predetermined electrical resistance connected across the buffer chip (see numbered paragraph 8 above, e.g.), so that the data bus latching circuit maintains or stores the level of data on the bus until a subsequent data or voltage level is driven onto the data bus In this way, different components of the computer system operating at different rates may

communicate over the data bus, i.e. the different rates may be "matched," while maintaining data integrity and allowing faster bus switching times.

Buch teaches that the bus may be a communication link between one or more computer components, and that the various components of the computer system may be "nodes" comprised of large scale integrated circuits or chips (see column 1, lines 14-39, e.g.), but does not specifically teach that the large scale integrated circuits or chips or components of the system are comprised of a digital signal processor (DSP) and a complex programmable logic device (PLD) having different rates at which they operate in performing their respective functions than that of the CPU. However, Bush does teach that the components may comprise any typical components used commonly with data buses (see column 3, line 56 to column 4, line 5, e.g.), and it would have been readily obvious to a person of ordinary skill in the art at the time the claimed invention was made to utilize commonly used large scale integrated circuit components or chips such as a digital signal processor and complex programmable logic device as circuit components or chips in Buch, so that the data bus latching or memory circuits may be used to maintain or store values on the data bus and allow appropriate communication between the different chips. It would have been obvious to use such data bus latching circuits because Buch teaches that delays due to "hand off" or transitions on the tri-state data bus may be avoided, thereby increasing bus utilization and data bandwidth, while also maintaining the integrity of the data on the bus to allow sampling by the different components, highly desirable features in a computer or communication system (note column 1, line 55 to column 2, line 64, e.g.).

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chiang et al is noted of interest as disclosing a bus hold or latch circuit including a pair of inverters, which form a non-inverting buffer, and a resistor connected across the buffer, similar to the present invention, and as also specifically teaching using such a data bus hold or latch circuit with programmable logic devices (PLDs) such as complex PLDs (CPLDs) as in the present invention (see column 1, lines 13-54 and Fig. 1, e.g.).

Warner is cited of interest as also teaching the use of a data bus circuit including a non-inverting buffer and a resistor coupled to a bus line similar to the present invention (see buffer 14 and resistor 16 in Fig. 3A, e.g.).

Meng et al is cited as disclosing a bus hold or latch circuit including a tristate buffer, similar to the present invention.

Kertis is cited as disclosing a "self-locking" load circuit for use in a computer or memory system similar to the present invention.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187